ASML

ASML's NXE platform for volume production

Semicon West

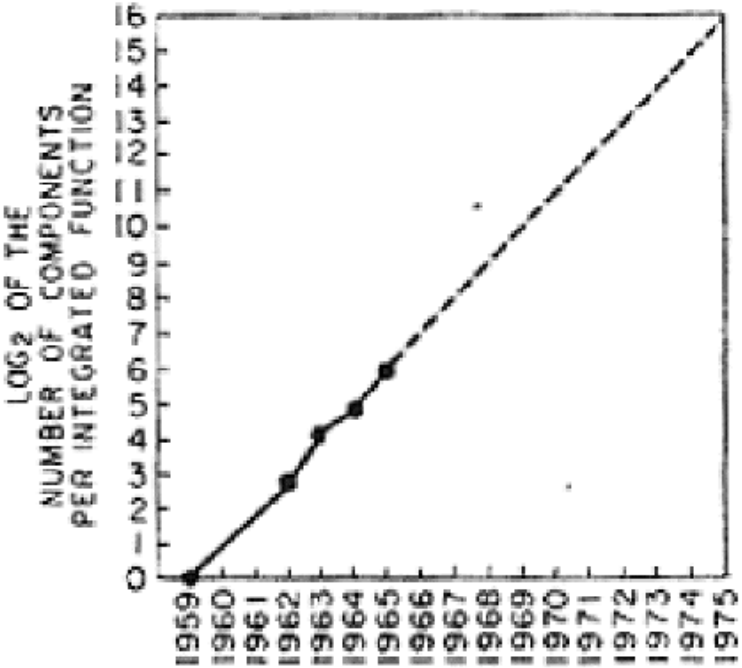
July 10th, 2013

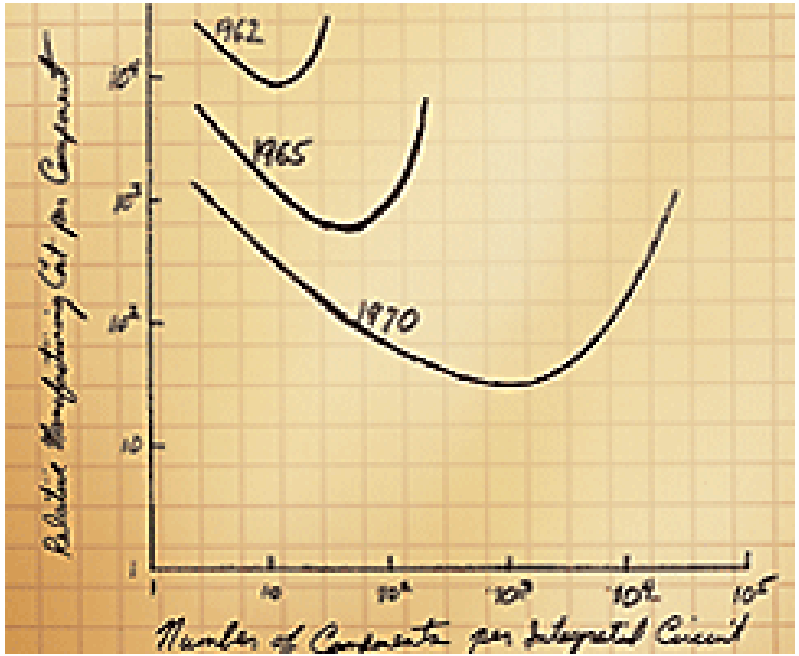
Skip Miller

Outline

- Why EUV
- EUV roadmap & scanner status
  - Roadmap
  - Performance status
  - Industrialisation status
- Summary

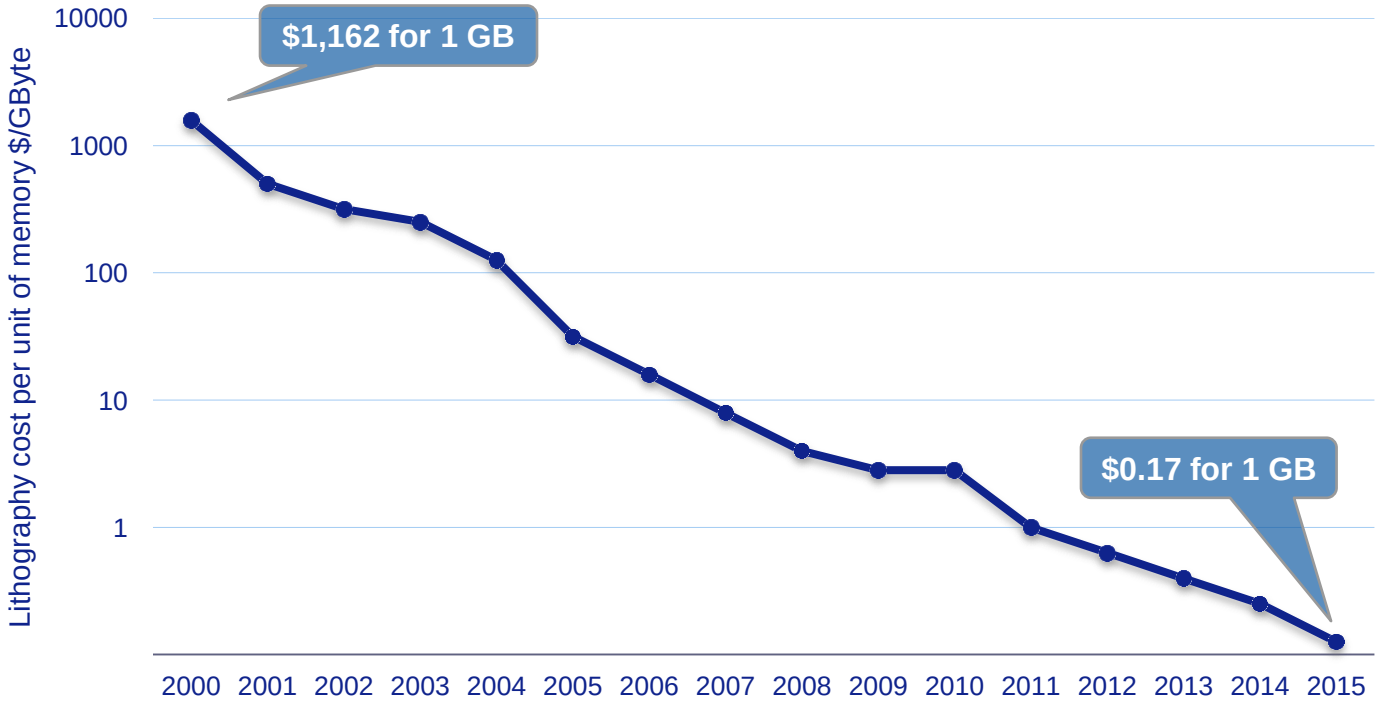
Moore's law : *Doubling of components per chip every 12 months resulting in a lower cost per component*





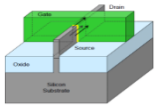
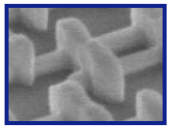
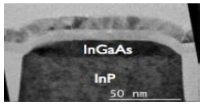
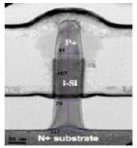
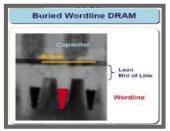
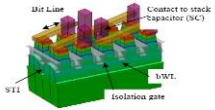
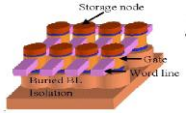
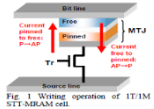
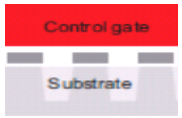
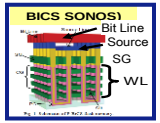
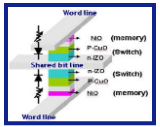
"Cramming more components onto integrated circuits", *Electronics Magazine April 19, 1965*

Moore’s Law: what it means for consumers



Source: Gartner. High quality Flash

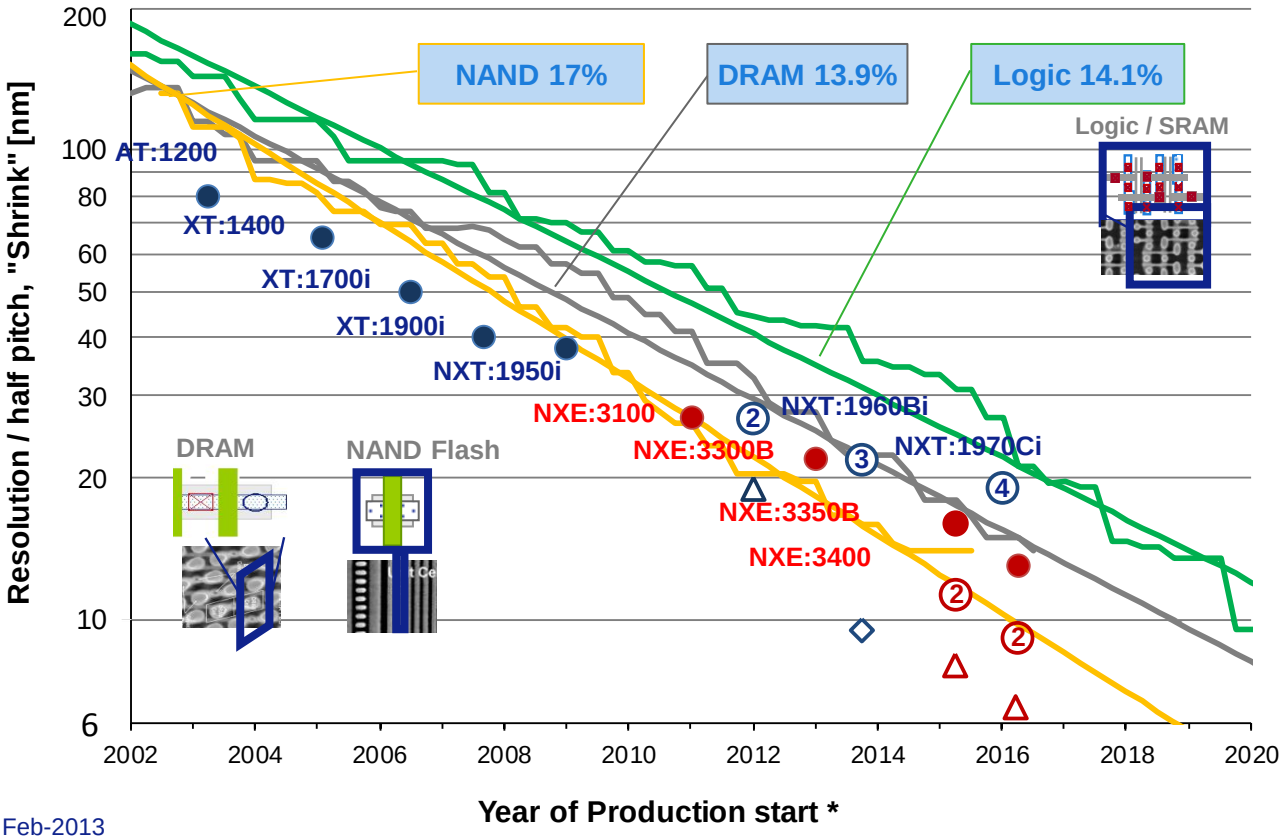
IC manufacturers' roadmaps supports further device scaling

	2012 - 2013	2014 - 2015	2016 - 2017	2018 - 2019
Logic	**22 - 20nm node** **Memory:** 0.09um2, SRAM **Device:** planar or FinFET (Intel) **Gate:** RMG-HKM **Channel:** Si **Vdd:** 0.8V 	**16 - 14nm node** **Memory:** 0.08um2 SRAM **Device:** FinFET, FDSOI **Gate:** RMG-HKMG **Channel:** Si; (Si)Ge **Vdd:** 0.6V 	**11 - 10nm node** **Memory:** 0.06um2 SRAM **Device:** FinFET **Gate:** HKMG **Channel:** Si, Ge, IIIVr **Vdd:** 0.5V 	**8 - 7nm node** **Memory:** FBRAM, STT-RAM, >8TSRAM **Device: FinFET,** Nanowire, TFET **Gate:** HKMG **Channel:** IIIV-Graphene 
DRAM	**38 - 32nm node** **Memory:** stacked MIM **Peri:** planar **Array:** 6F2, bWL **Gate:** poly/SiO2 **Channel:** Si **Vdd**=1.35V 	**29 - 22nm node** **Memory:** stacked MIM **Peri:** planar HKMG **Array:** 6F2, bWL **Gate:** HKMG **Channel:** Si **Vdd**=1.2V 	**22 - 16nm node** **Memory:** stacked MIM **Peri:** planar **Array: 6F2,** 4F2, bBL, LBL, 1T1C(VFET) **Gate:** HKMG **Channel:** Si **Vdd**=1.1V 	**16 - 14nm node** **Memory:** FBRAM, STT-MRAM, RRAM, PcRAM **Peri:** planar **Array:** 4F2, 1T, 1T1R, 1T1MTJ(VFET) **Gate:** HKMG **Channel:** Si **Vdd**~1V 
Flash	**19 - 16nm hp** **4.5F - 6F2 asymm. cell** **Density:** 128G **Device:** FG 	**16 - 13nm hp** **3D NAND intro at 5x → 4xnm** **6F2 asymmetric cell** **4F2 symmetric cell** **Density:** 256-512G **Device:** dual-FG 	**~ 11nm hp (planar)** **3D NAND at 3x → 2xnm X-pt intro at 2xnm** **7F2 asymmetric cell** **4F2 symmetric cell** **Density:** 512-1024G **Device::** dual-FG**,** BiCS in HVM(@4xnm)	**< 10nm hp (planar)** **X-pt intro at 2xnm** **Density:** > 1T with 3D chip stacking **Device:** 3D BiCS, XPoint-RRAM **Selector:** diode 

Source: IMEC, ASML TDC, Jan 2013

Industry roadmap towards <10 nm resolution

Lithography roadmap supports continued shrink



- Single Exposure
- 2D LE^n Patterning
- 1D SADP
- 1D SAQP
- DUV
- EUV

LE = Litho-Etch, n = number of iterations

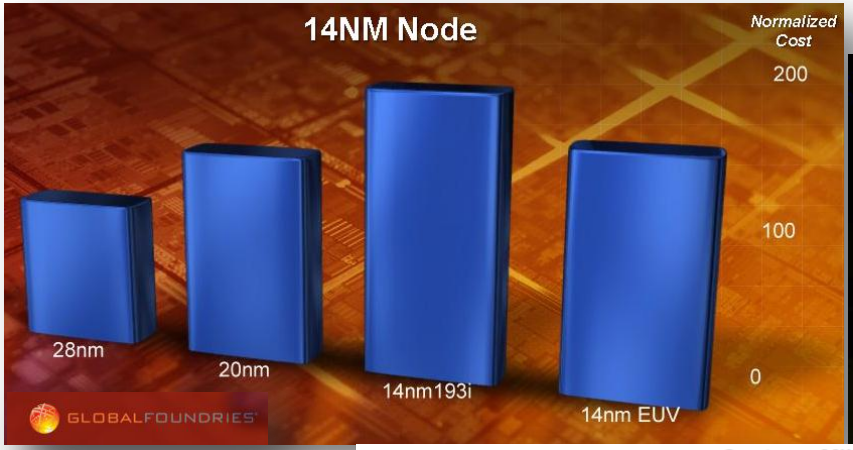
SADP = Self Aligned Double Patterning

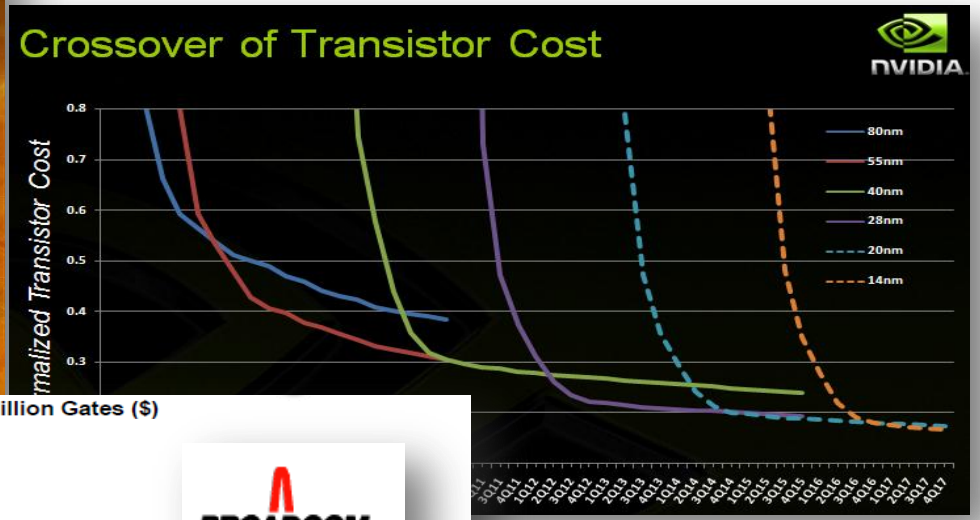
SAQP = Self Aligned Quadruple Patterning

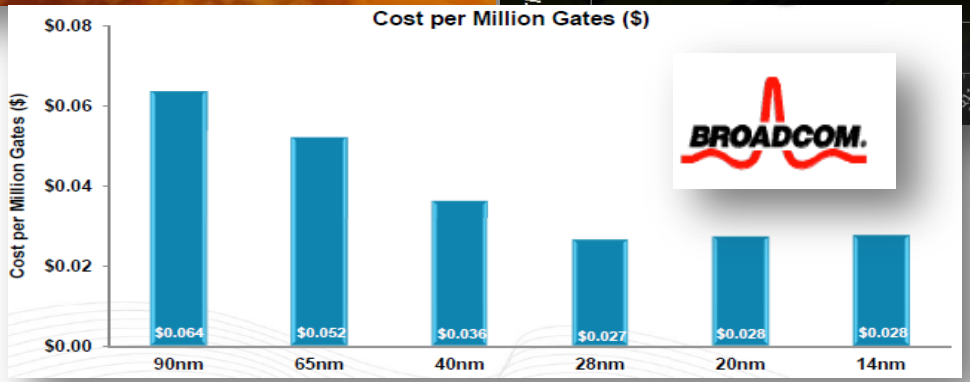
* Note: Process development 1.5 ~ 2 years in advance

Feb-2013

Cost becomes a concern post 28 nm



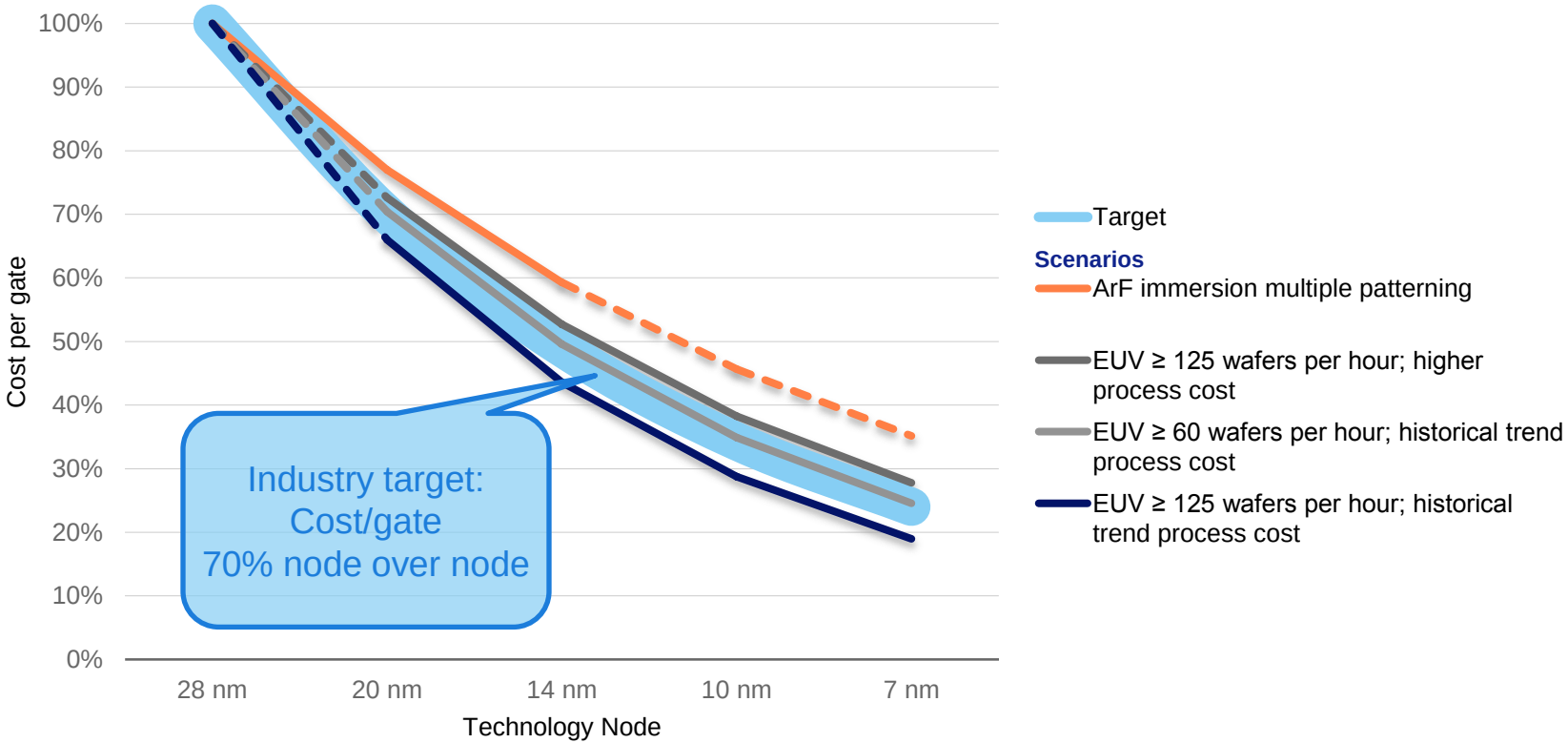




Sources: nVidea, ITPC, nov, 2011
Broadcom, IMEC, may 2012
GF, ISS, jan 2013

Litho roadmap supports cost per gate roadmap

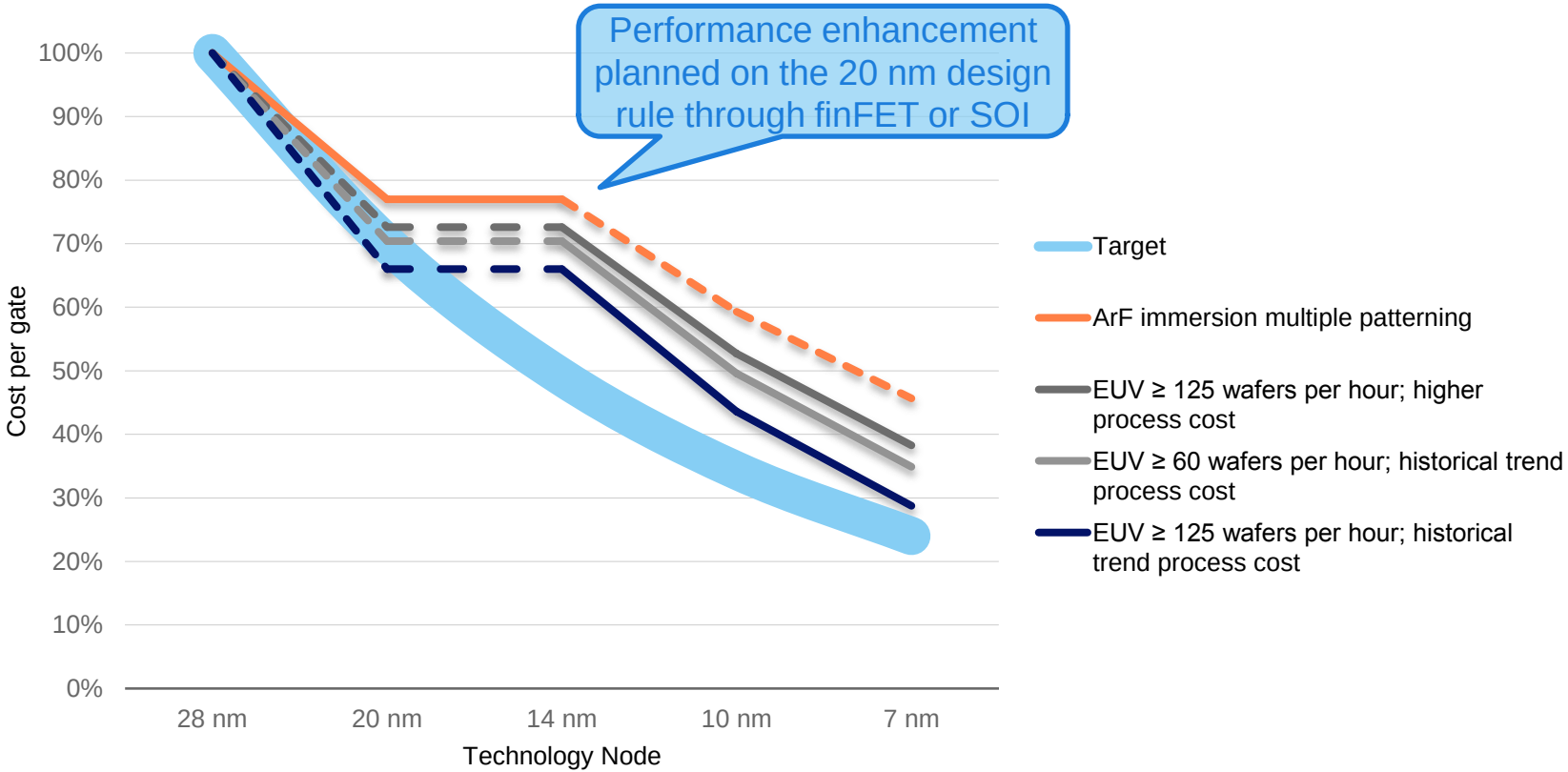
EUV needed to enable industry target



Source: ASML

Litho roadmap supports cost per gate roadmap

EUV needed to enable industry target



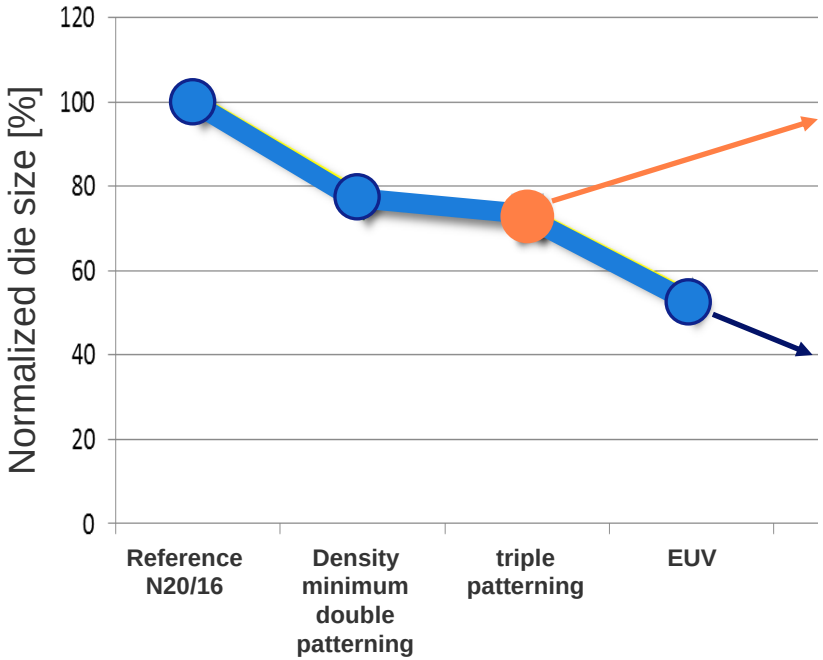
Source: ASML

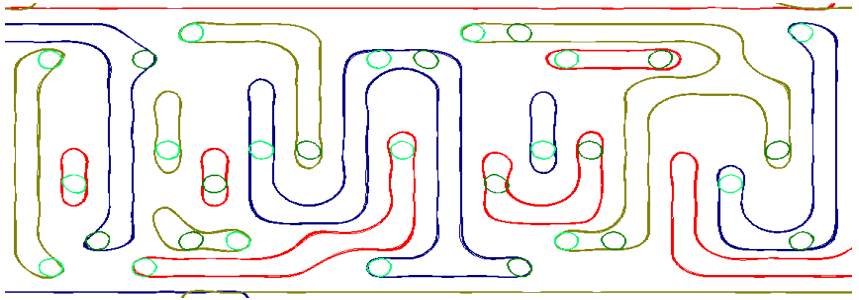
28nm **20nm** **finFET@ 20 nm** **14nm** **10nm**

Fin FET scaling reset

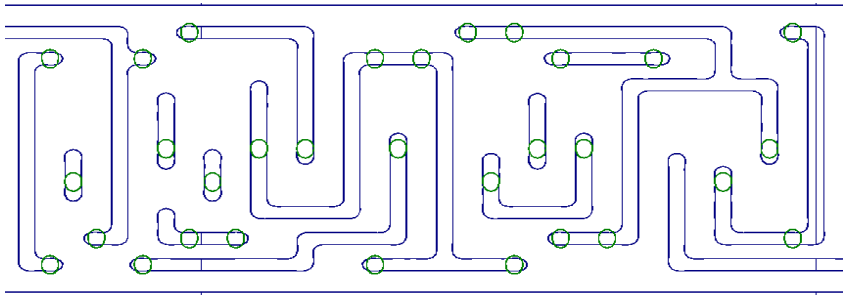
Only EUV can enable 50% scaling for the 10 nm node

Layout restrictions and litho performance limit shrink to ~25% using immersion





Triple patterning does not show an process window



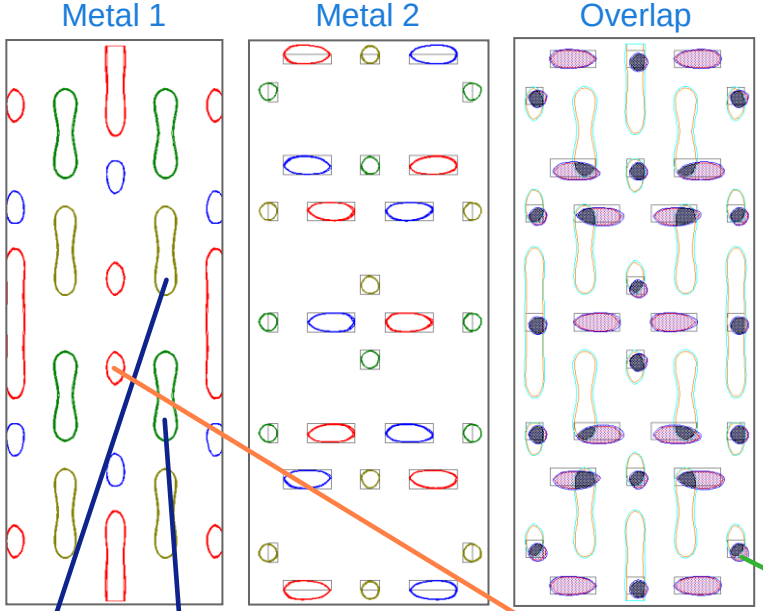
EUV meets all litho requirements

Source: ARM, Scaled N20 nm flip-flop design

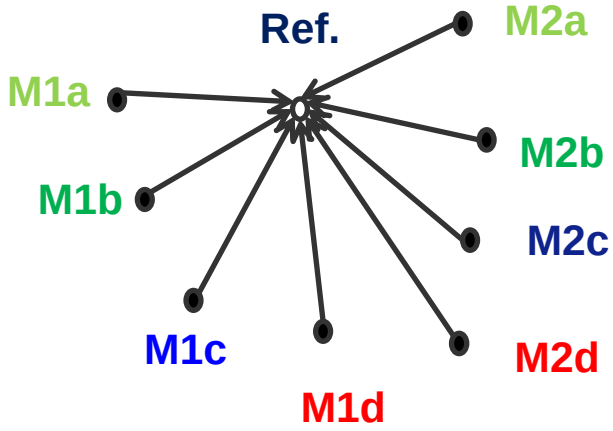
Even gridded SRAM designs prefer EUV at 10 nm

Limited overlay between local interconnect layers makes multiple patterning very difficult

Quadruple expose immersion



All exposures have to match to each other to enable sufficient Metal 1 to 2 overlap, leading to tight overlay requirements



1) Small overlapping process window

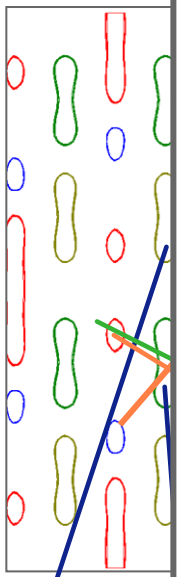
2) Marginal CD control

3) Failing overlap at 3 nm overlap

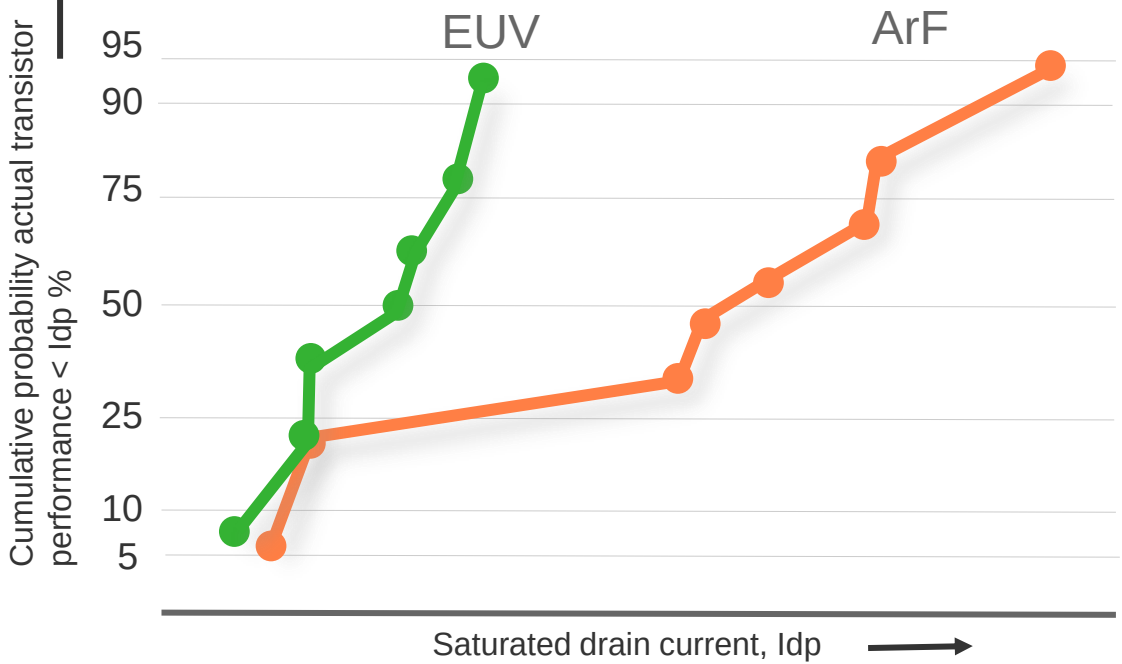
Even gridded SRAM designs prefer EUV at 10 nm

Limited overlay between local interconnect layers makes multiple patterning very difficult

Metal 1

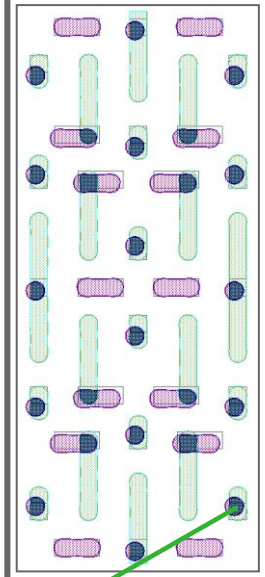


Integrated transistor performance on EUV superior compared to ArF double pattering



Source: Sam Sivakumar, Intel, SPIE, Feb 2013

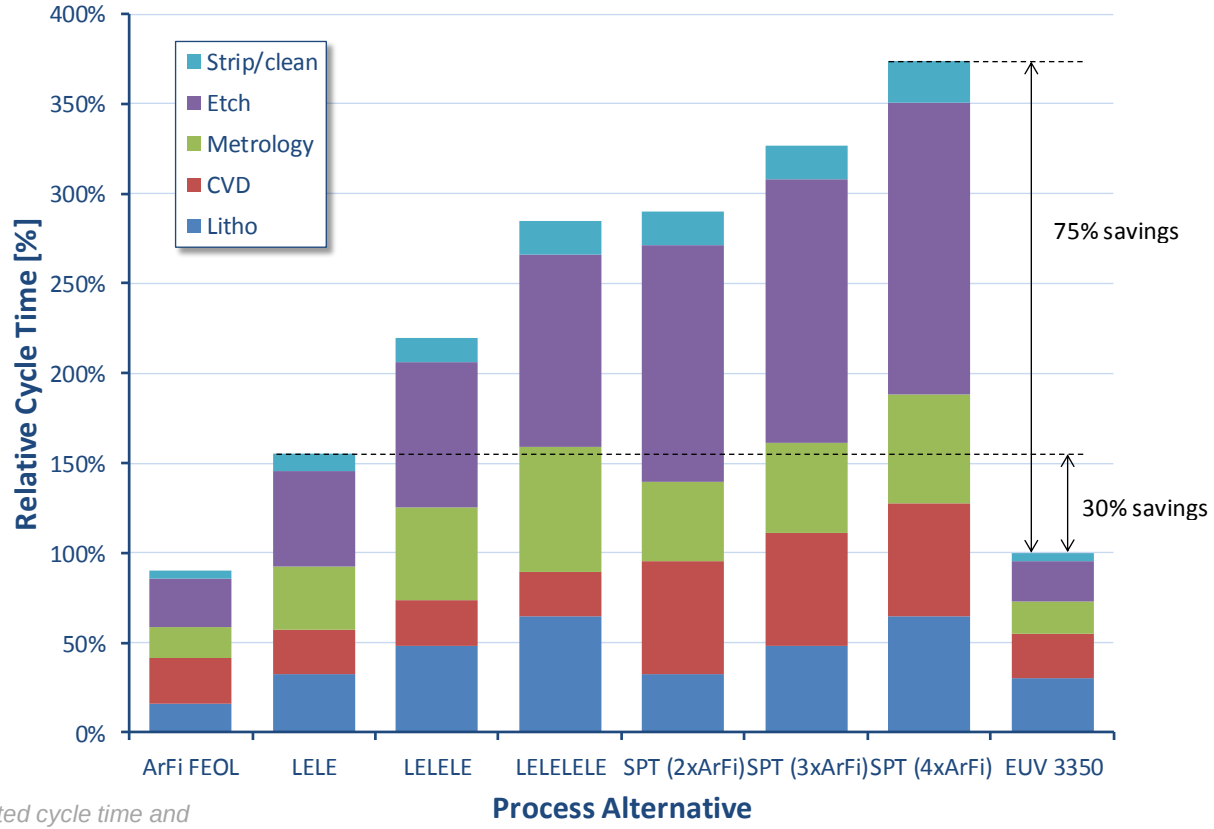
Overlap



1) Enlarg
pr

o vs
ay

EUV gives 30-75% lower cycle time than multi-patterning



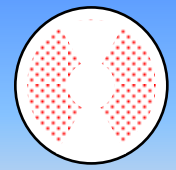
Analysis based on estimated cycle time and Pollaczek-Khinchine queuing theory with experimental data on arrival rate variations

Outline

- Why EUV
- **EUV roadmap & scanner status**
  - **Roadmap**
  - **Performance status**
  - **Industrialisation status**
- Summary

NXE technology roadmap has extendibility to <7nm

					Under study			
Resolution [nm]	**32**	**27**	**22**	**16**	**13**	**10**	**7**	**<7**
Wavelength [nm]	13.5							
Lens – NA	0.25		0.33			0.33NA DPT		0.45-0.60 DPT
Lens – NA						0.45	0.60	
Lens – flare	8%		6%	4%				
Illumination – coherence	σ=0.5	σ=0.8	σ=0.2-0.9	Flex-OAI	Extended Flex-OAI			
Illumination – coherence					reduced pupil fill ratio			
Overlay – DCO [nm]	7	4.0	3.0	1.5	1.2	1.0		
Overlay – MMO [nm]	-	7.0	5.0	2.5	2.0	1.7		
TPT (300mm) – Dose [mJ/cm^2]	5	10	15	15	20	20		
TPT (300mm) – Power [W]	3	10 - 105	80 - 250	250	250	500		
TPT (300mm) – Throughput [w/hr]	-	6 - 60	50 - 125	125	125	165		



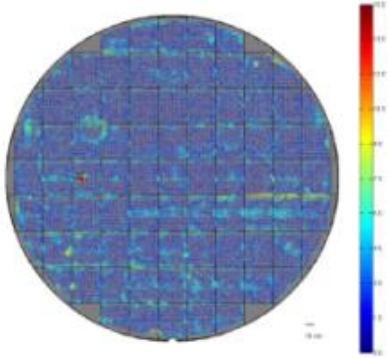
pupil fill ratio defined as the bright fraction of the pupil

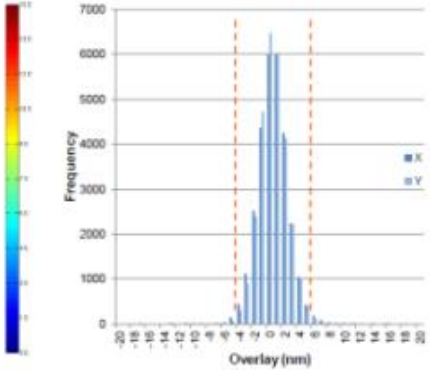
ASML's NXE:3100 and NXE:3300B

	NXE:3100	NXE:3300B
NA	0.25	0.33
Illumination	Conventional 0.8 σ	Conventional 0.9 σ Off-axis illumination
Resolution	27 nm	22 nm
Dedicated Chuck Overlay / Matched Maching Overlay	4.0 nm / 7.0 nm	3.0 nm / 5.0 nm
Productivity	6 - 60 Wafers / hour	50 - 125 Wafers / hour
Resist Dose	10 mJ / cm2	15 mJ / cm2

Good overlay on NXE:3100 at customers

NXE:3100 BEST ACHIEVABLE MEASURED OVERLAY





X: |Mean|+3σ: 6.0nm
Y: |Mean|+3σ: 5.6nm

Reference grid from NXE:3100, second layer on XT:1900i
1 wafer, 83 fields, 26x33mm², 17x22 pts/field

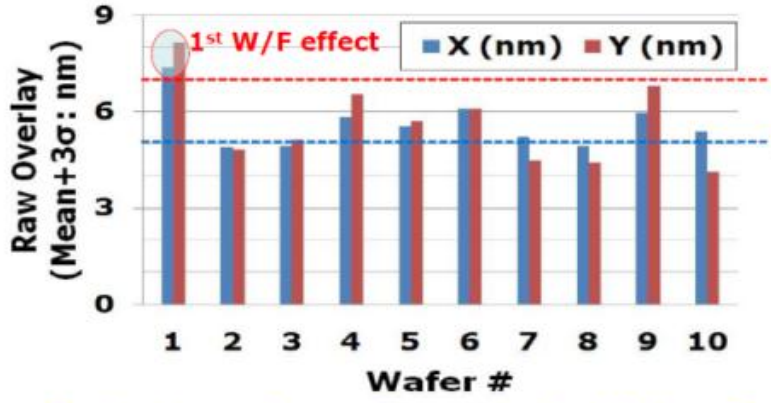
Applying 10-parameter, CPE and iHOPC corrections, brings measured overlay down to 6nm |Mean|+3σ

imec

Matched Product Overlay Trend

EUV Symposium (2011, Oct.)

10 wafer exposure



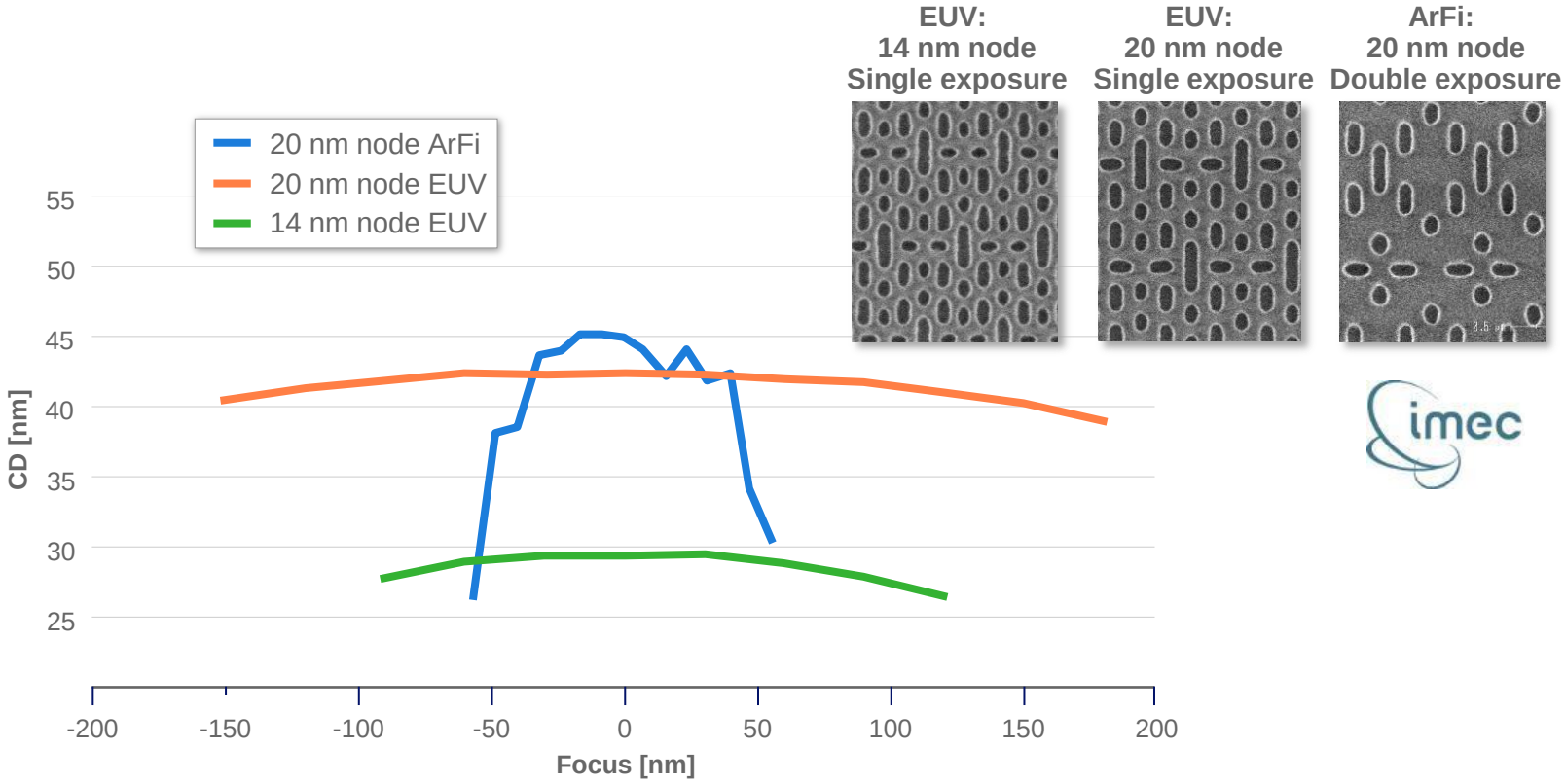
- Product overlay can be controlled below 7nm
- 1st wafer effect & wafer variation under investigation

hynix

18

Large process windows measured on the NXE:3100

Down to 14 nm node SRAM M1 layer



Eleven NXE:3300B systems in various states of integration new clean room completed in July ‘12

System 1

Development tool

System 9

System 2

System 6

New cleanroom

System 3

System 7

System 4

System 5

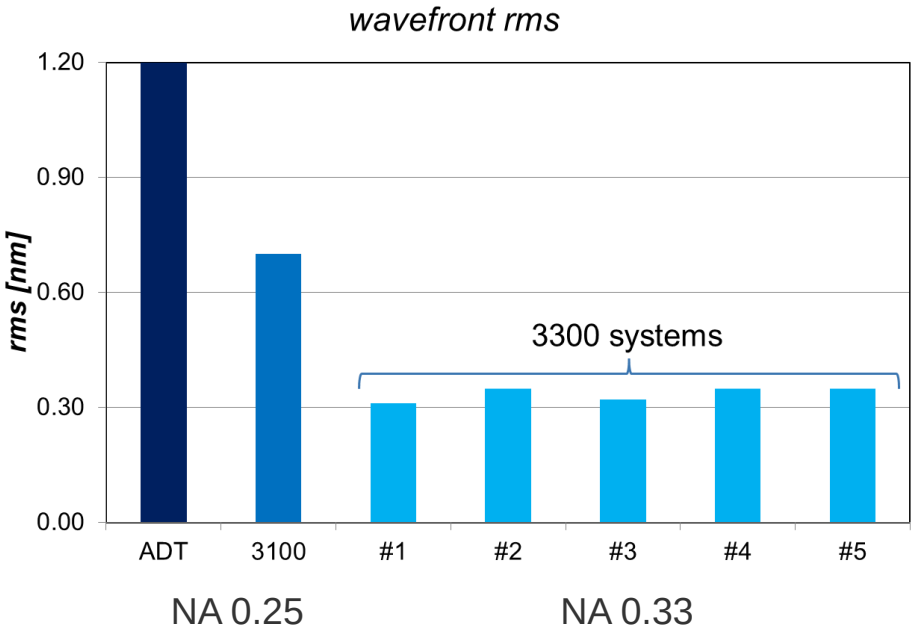
System 8

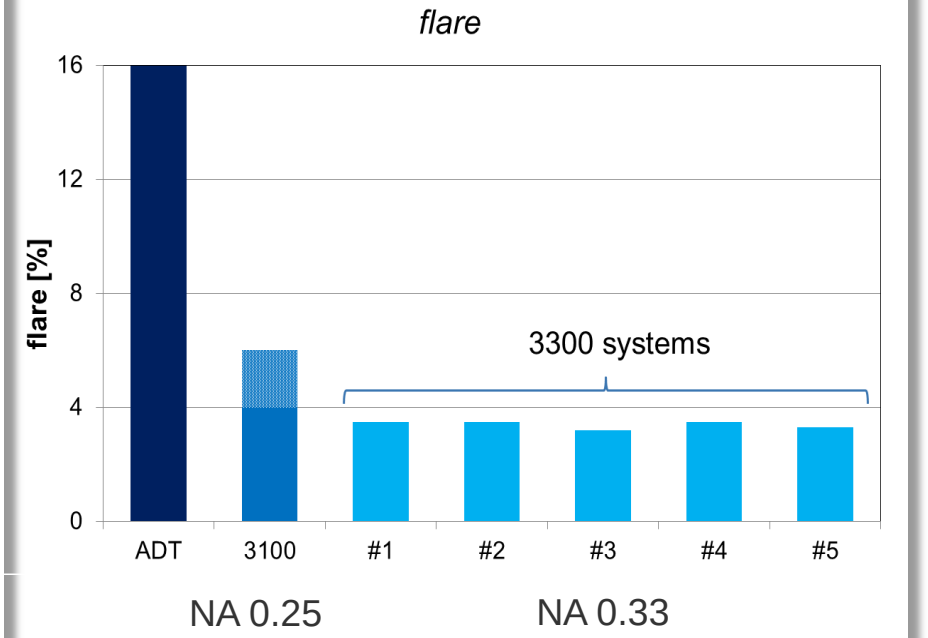
System 10
Training

System 11

Consistent performance of 0.33 NA lens

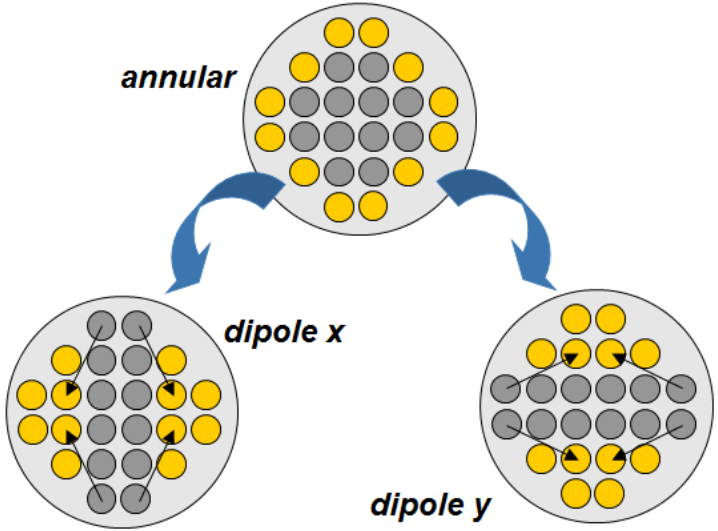
Wavefront error improved by a factor of 2 from 0.25NA lens

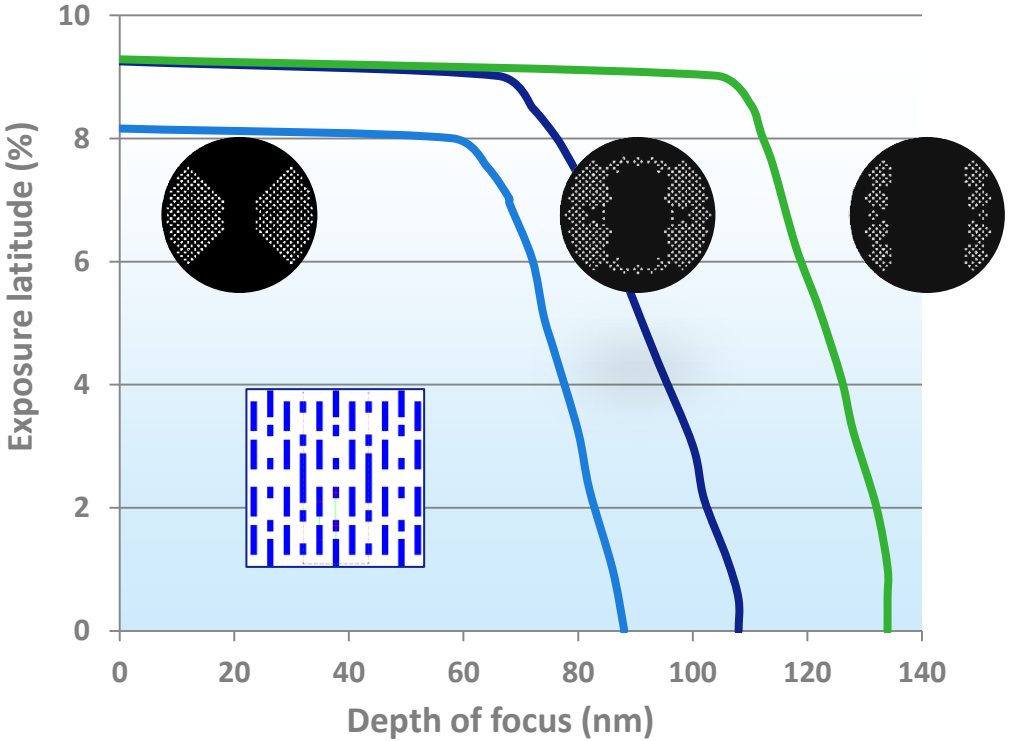




Presentation: Martin Lowisch (Zeiss SMT AG)

The NXE:3300B offers new concept off-axis illumination to enhance process window

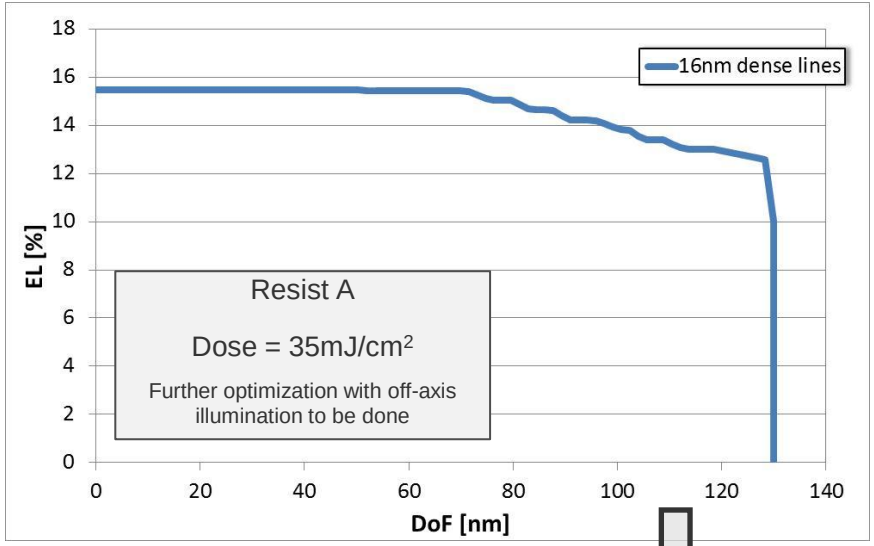


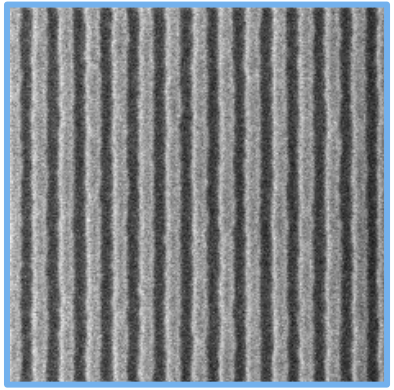


Simulations by Tachyon SMO NXE

Presentation: Martin Lowisch (Zeiss SMT AG)

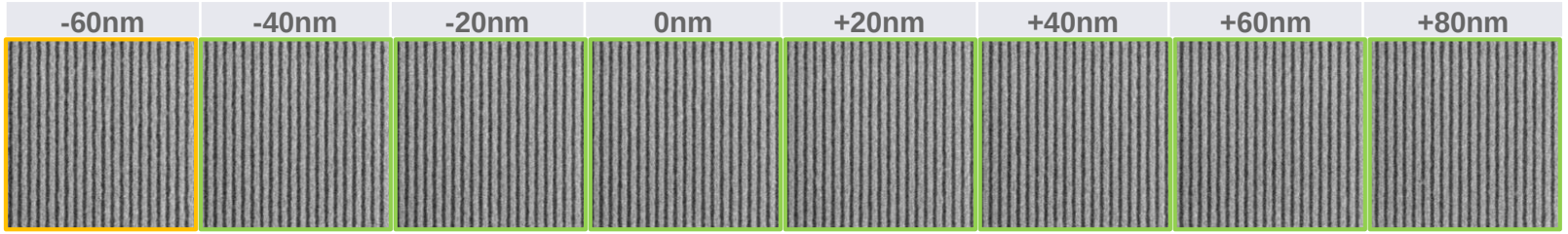
16nm dense lines with >15% exposure latitude and >120nm DoF on NXE:3300B (dipole-45 setting)





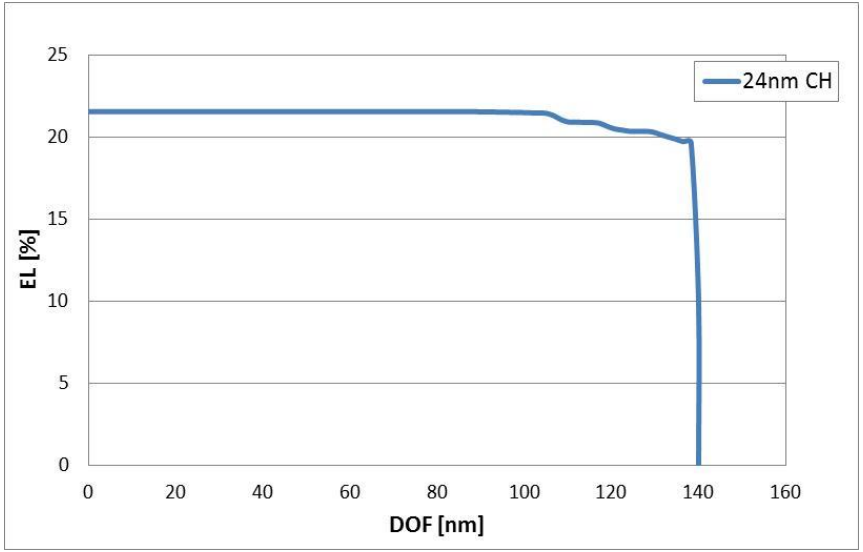
16nm L/S Dipole 45X
29.0mJ/cm2
Resist B

imec

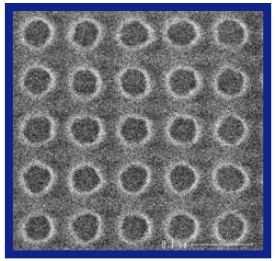


24nm regular Contact Holes (DRAM 1x node) with Exposure Latitude >20%, and DOF >120nm

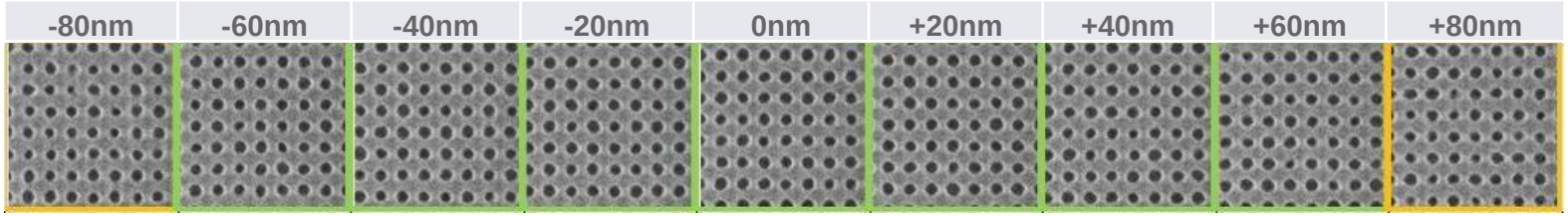
Single exposure
Conventional setting



LCDU = Hole-to-hole variation over 25 CHs [nm 3σ]

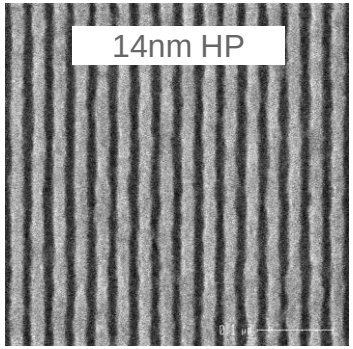


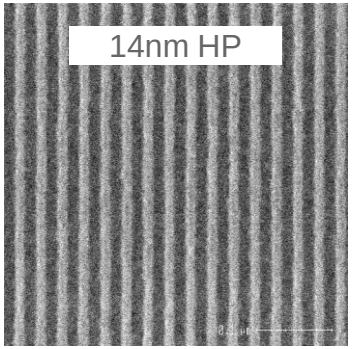
Resist A
26mJ/cm²

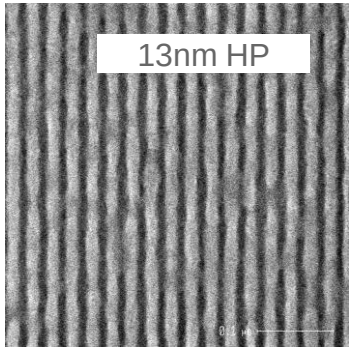


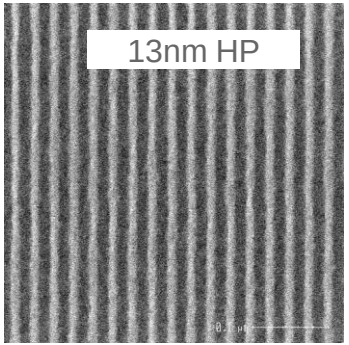
LCDU [nm 3σ]	-80nm	-60nm	-40nm	-20nm	0nm	+20nm	+40nm	+60nm	+80nm
	4.0	3.6	3.2	2.9	2.8	2.9	3.2	3.2	3.8

Resolution shown on NXE:3300B for dense line spaces, regular and staggered contact holes; all single exposures







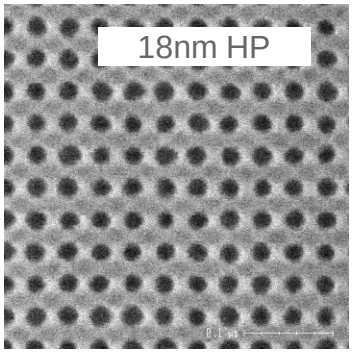


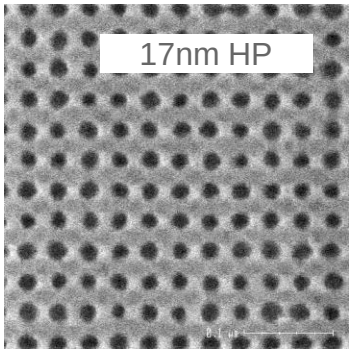
Dipole30,

Chemically Amplified Resist (CAR)

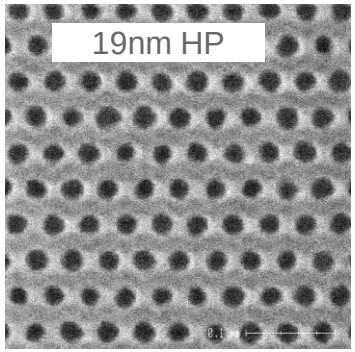
Dipole45,

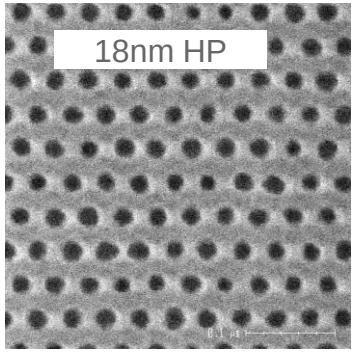
Inpria Resist





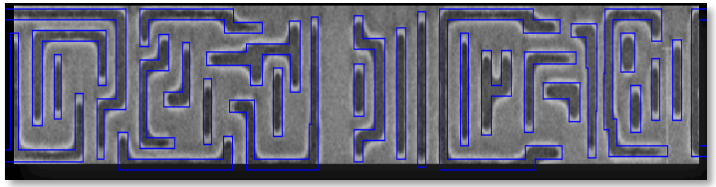
Quasar 30 (CAR)

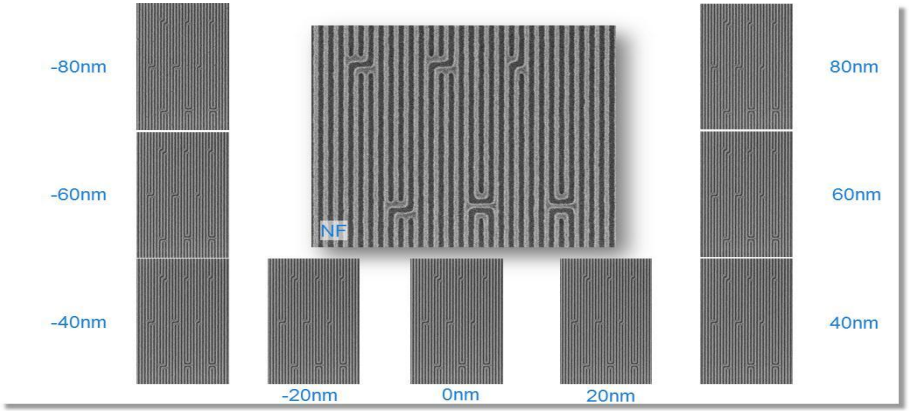




Large Annular (CAR)

EUV enables single exposure 10 nm node

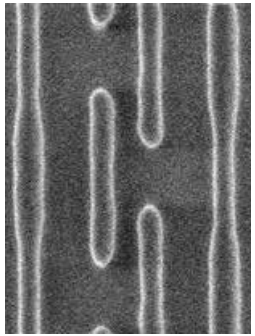




10nm node M1 clip, 23nm half pitch, exposed on an NXE:3300B with conventional illumination. Clip courtesy of ST

EUV	ArFi
Single exposure shows good resemblance between reticle and wafer layout	Requires multiple patterning
Best HV focus difference <10nm	Best HV focus difference up to 60nm
Measured UDoF > 100nm	Typical UDoF ≈ 50nm

SRAM 2D features: 42nm Tip2Tip performance

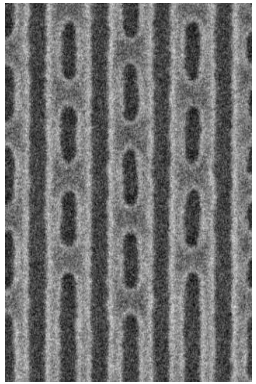


imec

ArFi 28nm node SRAM 90 pitch

Tip2Tip distance (CD) = 80nm

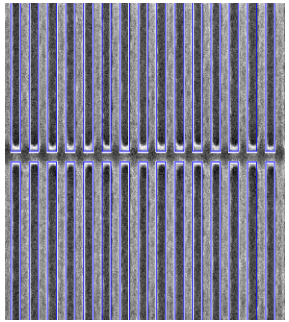
Interfield CDU = 8nm



EUV 10nm node SRAM 44nm pitch

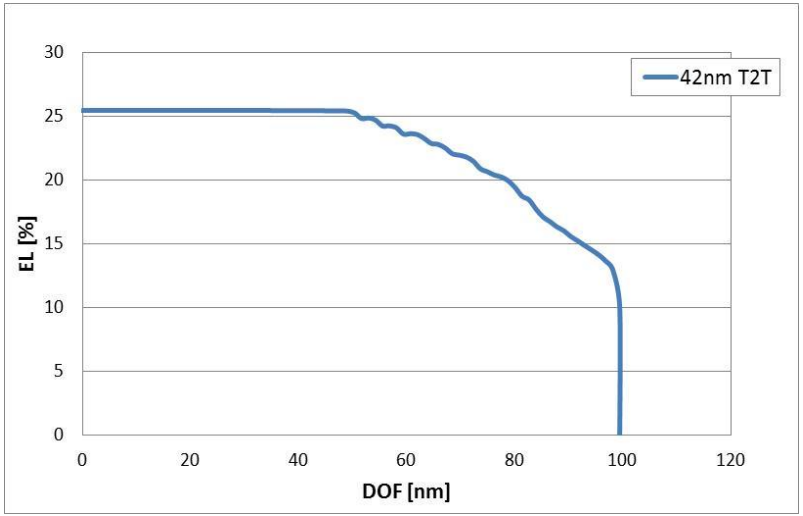
Tip2Tip distance (CD) = 42nm

Intrafield CDU = 1.3nm



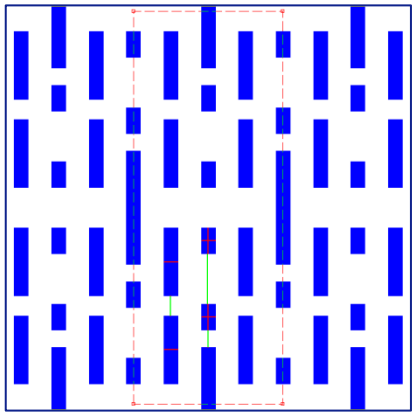
Process Window of line-ends with

Tip2Tip CD=42nm



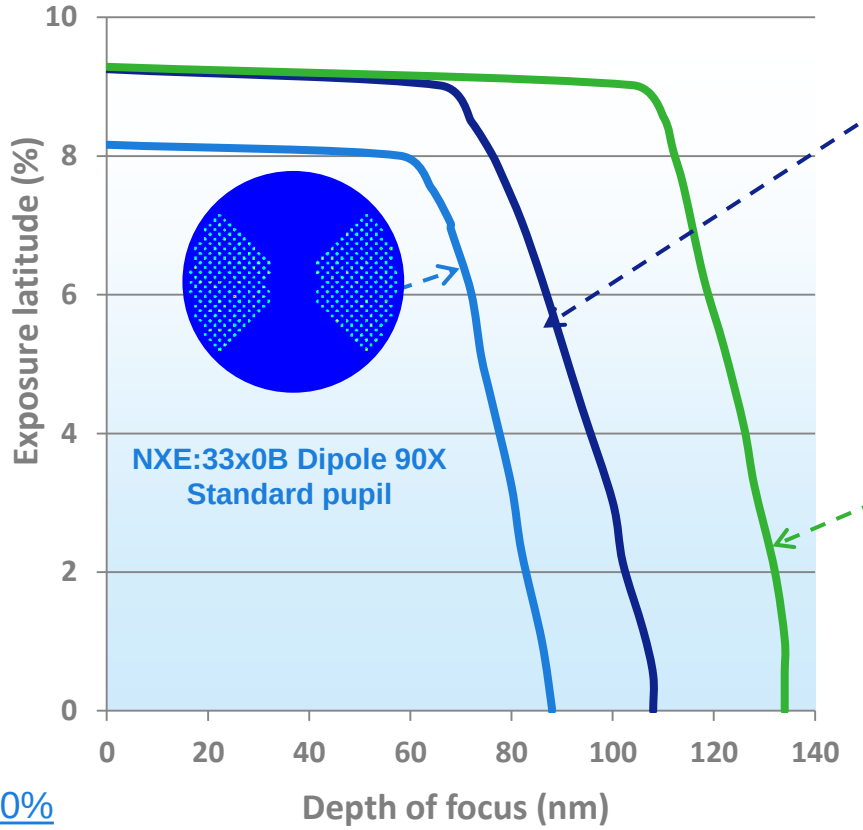
EUV extendable to 7 nm node through holistic approach

Source mask optimization at 0.33 NA and reducing the pupil filling to 20% maintaining full productivity using Tachyon SMO



Logic 7 nm node

- Local interconnect layer
- Bright field
- Feature width = 12 nm
- Feature pitch = 32 nm

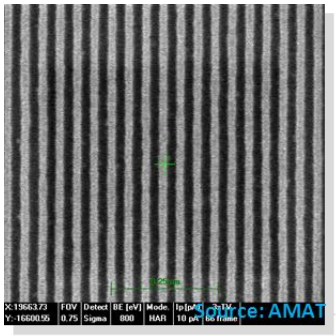


Depth of Focus (DOF) at 8%;
Exposure Latitude increased ~100%

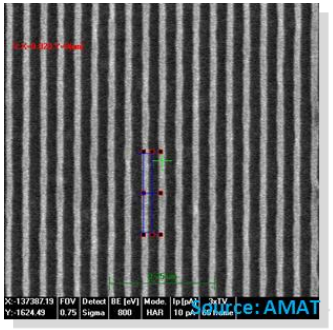
NXE:3300B shows single-digit (9 nm HP) patterning capability!

using spacer-assisted double patterning (SADP)

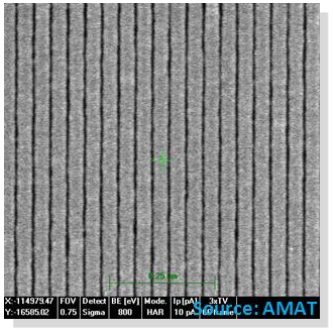
NXE litho
(single expose, 18nm HP)



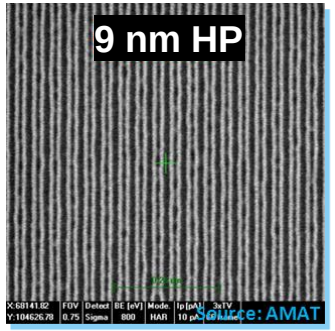
Core etch



Spacer dep.



Spacer etch



Demonstrated 9 nm half-pitch L/S pattern with EUV single SADP flow.

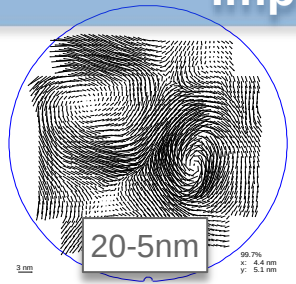
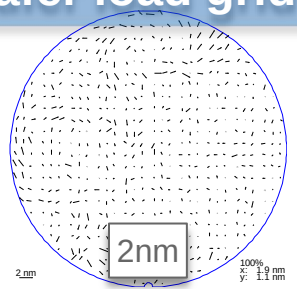
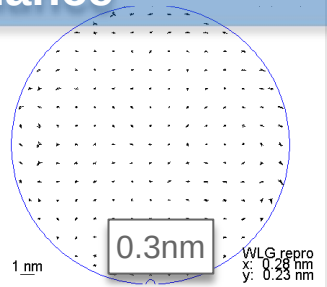
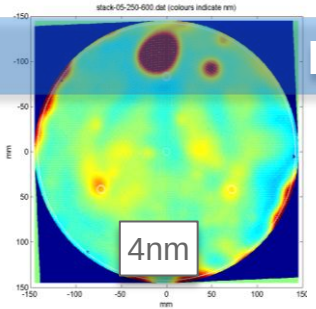
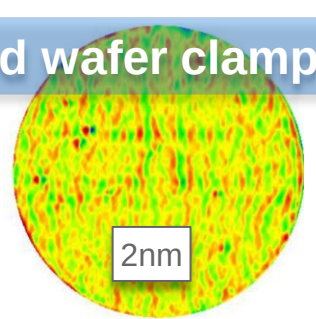
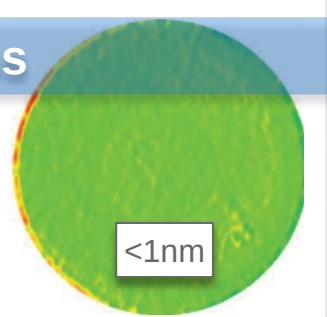
Litho Conditions:

- ASML NXE:3300B system
- EUVL single expose 18nm HP
- 0.33NA, Dipole-90x illumination
- Resist: 50nm EUV J1099 on 20nm BS AL412 UL on stack wafer with Hard mask

Source: ASML, IMEC, AMAT

NXE:3300B overlay improvements

Better wafer load grid performance and improved wafer clamp flatness

ADT	NXE:3100	NXE:3300B
Improved wafer load grid performance		
 20-5nm	 2nm	 0.3nm
Improved wafer clamp flatness		
 4nm	 2nm	 <1nm

Measured by repeatedly clamping a wafer

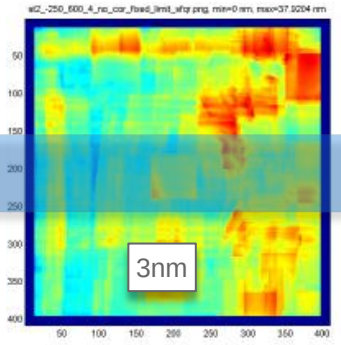
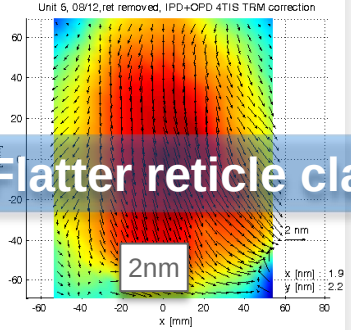
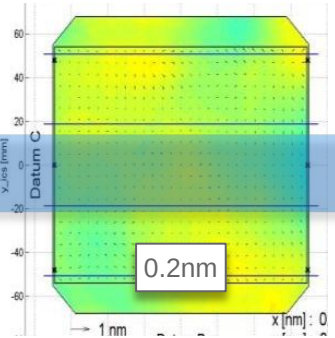
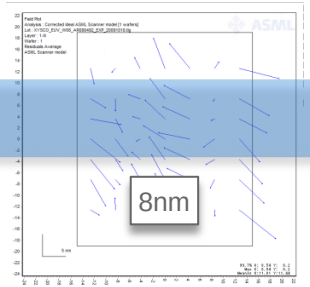
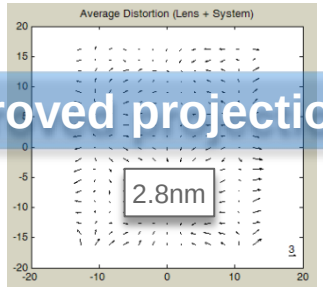
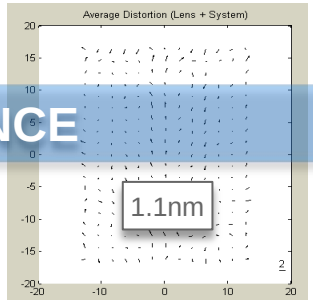
Measured heightmap with interferometer

Translated into overlay via model

Numbers show the contribution to overlay, budget is RSS of multiple components

NXE:3300B overlay improvements

Better lens performance and improved reticle clamp flatness

ADT	NXE:3100	NXE:3300B
		
		

Measured heightmap with interferometer

Translated into overlay via model

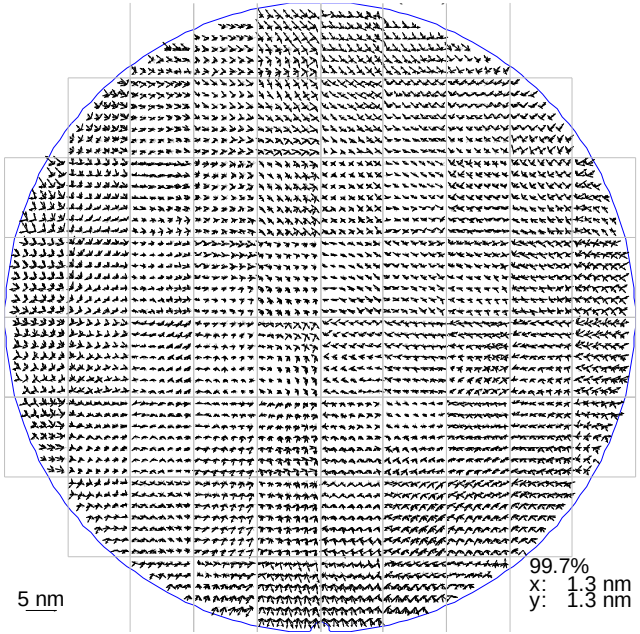
Flatter reticle clamps

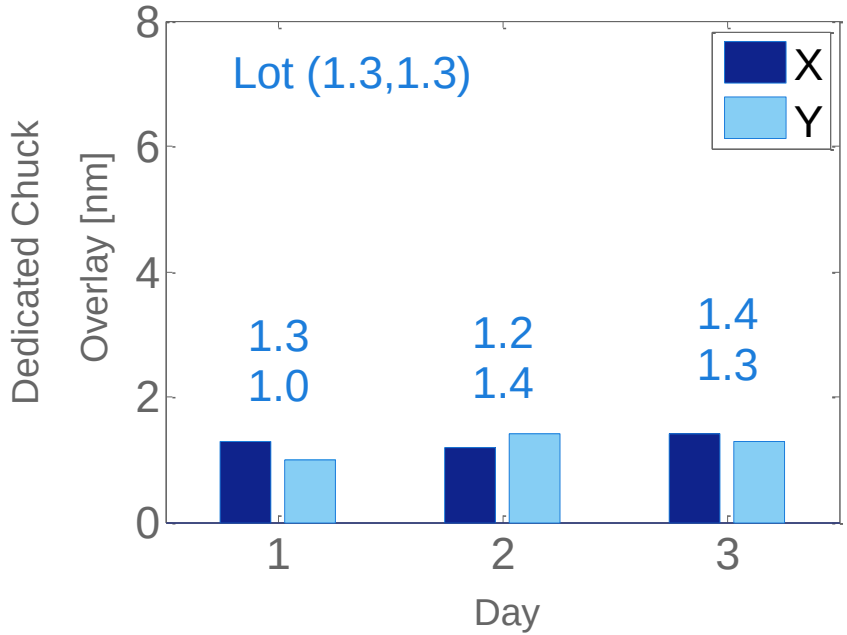
Improved projection lens NCE

Measured lens performance

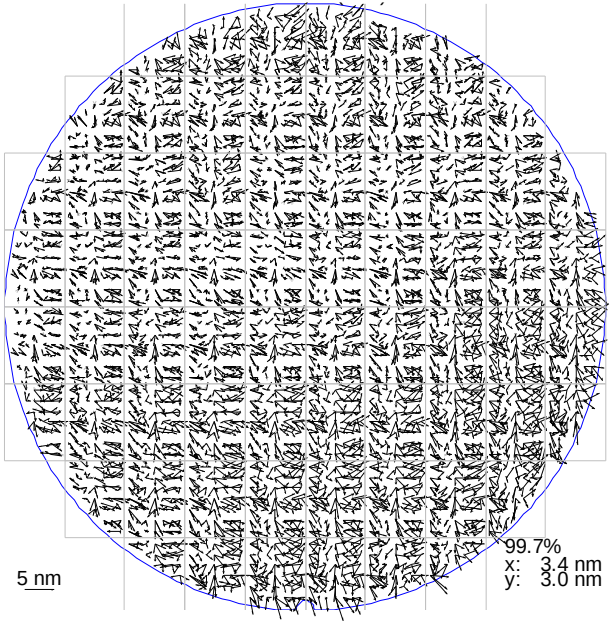
Numbers show the contribution to overlay, budget is RSS of multiple components

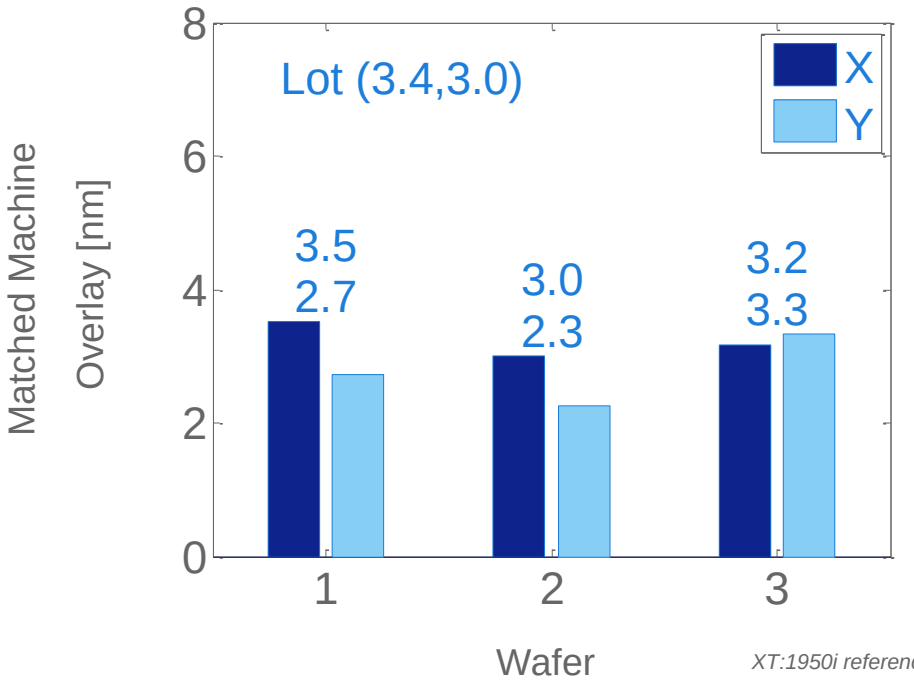
Full wafer dedicated chuck overlay of <1.4nm





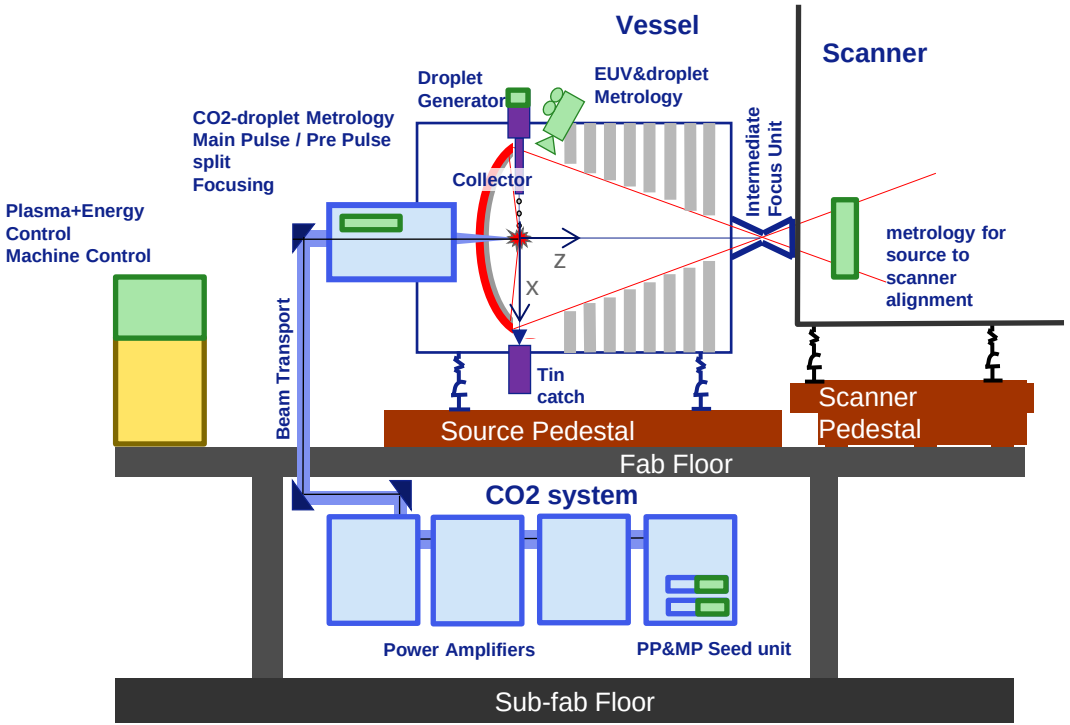
NXE-Immersion Matched Machine Overlay of <3.5nm





XT:1950i reference wafers
EEXY subrecipes
18par (avg field) +
CPE (6 par per field)

EUV source system cross-section



x=droplet stream direction, z=CO2 light direction, y=orthogonal

Key components:

- Drive Laser
- Droplet generator
- Vessel

Power

- Final Focus Assembly
- Collector

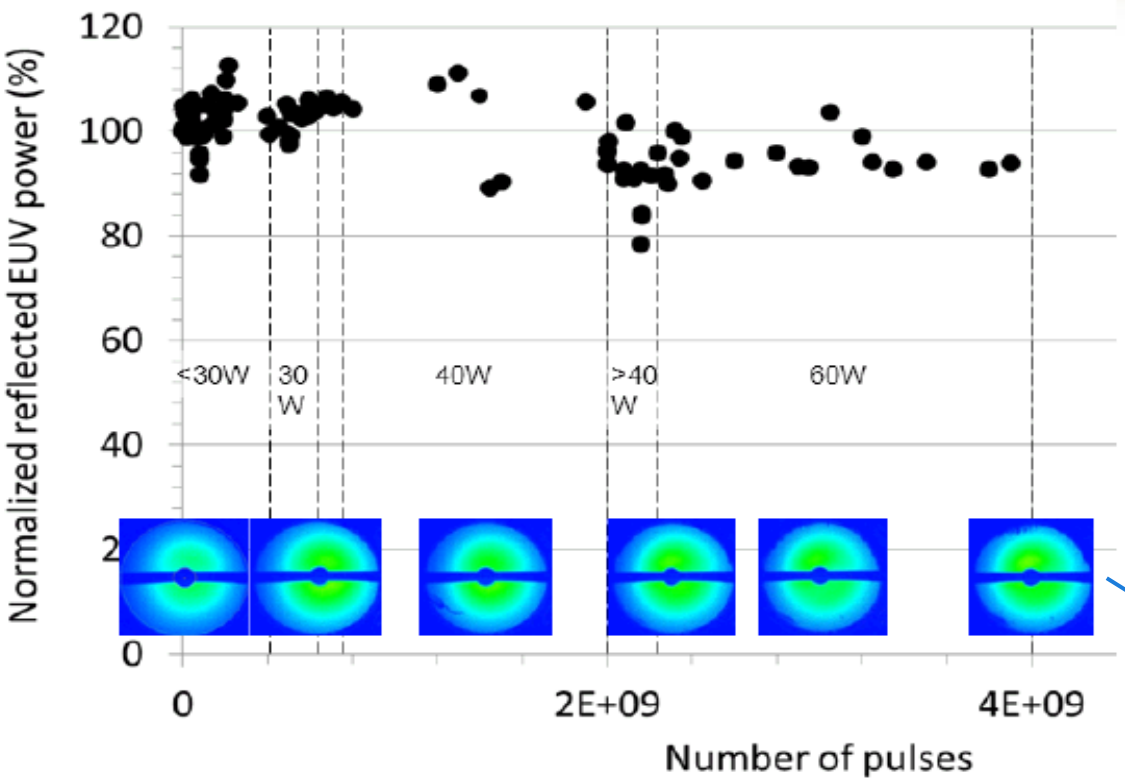
Availability

- Controls (E,x,y,z,t)

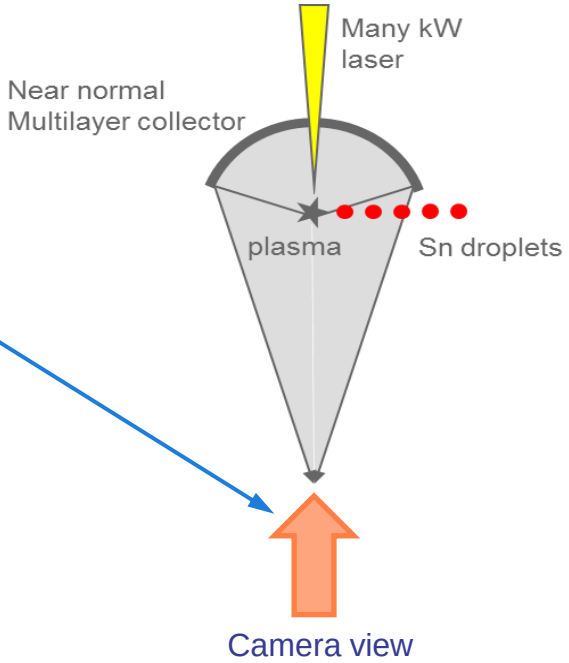
Dose control

EUV collector reflection stability

Collector performance over time required for system availability

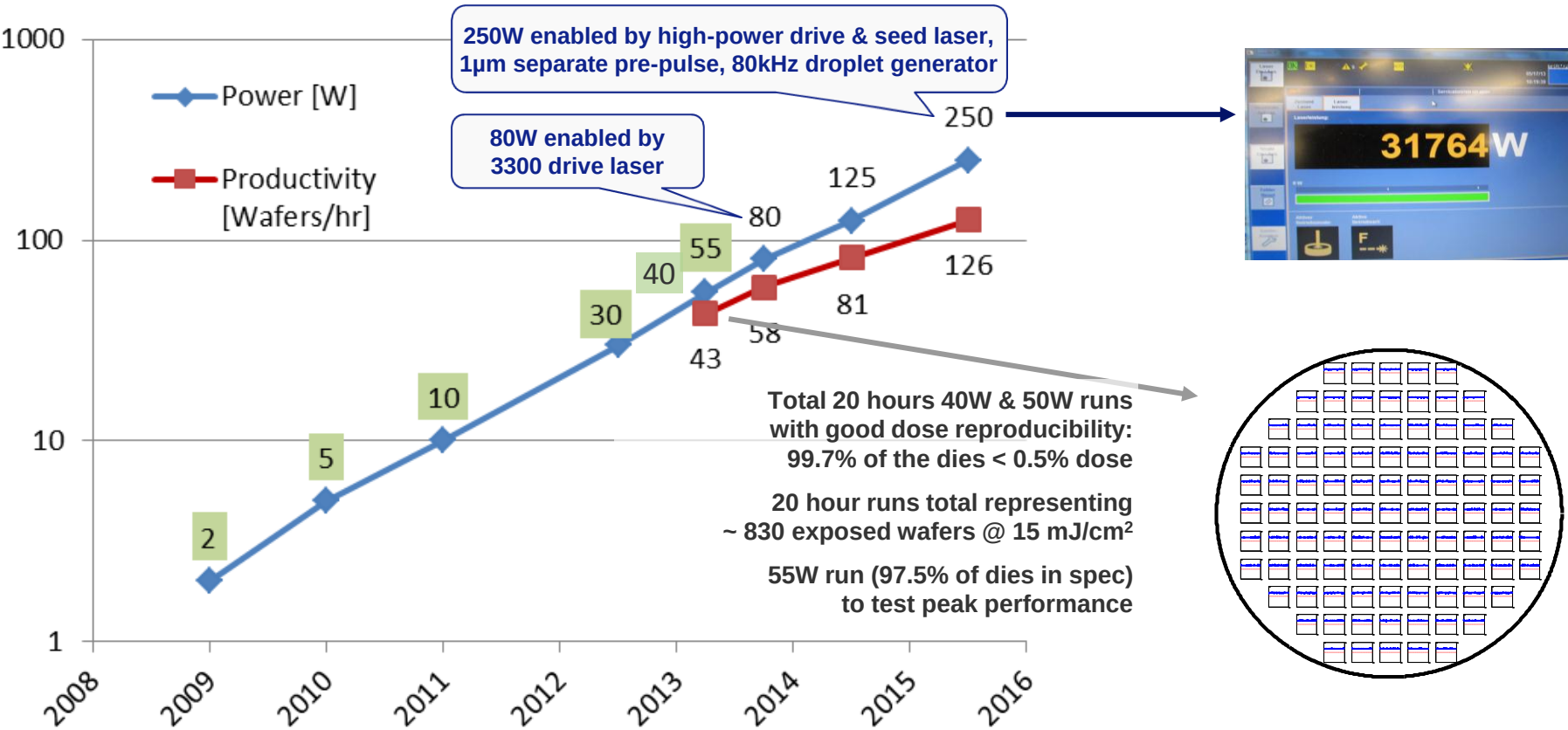


4 B pulses represent ~40hr continuous exposures.



EUV source: repeatable stable performance, dose in spec

250 W target to be reached in 2015



NXE:3300B systems have started shipping

Outline

- Why EUV
- EUV roadmap & scanner status
  - Roadmap
  - Performance status
  - Industrialisation status
- **Summary**

Summary : EUV production insertion for 10nm Logic and 1xnm DRAM volume Production in 2015~16 expected

- **EUV enables**
  - Continued Moore's law scaling for the next generation ICs
  - Cost effective Lithography, more efficient shrink & potential improvement in device performance
  - Cycle time reduction due to process simplification

- **EUV roadmap & scanner status**
  - NXE:3100 in use for process/device development at customers with positive results
  - NXE:3300B has started shipping and meets imaging and overlay targets
  - Resolution capability on LS & contacts at customer process node conditions demonstrated
  - Overlay performance of DCO<1.5nm and MMO<3.5nm demonstrated for production capability
  - Industrialization progress demonstrated towards 70 WPH in 2014
  - Further improvements are still required on scanner source power, resist, and mask
  - Roadmap to <7nm with 0.33NA + extensions, double patterning &/or higher NA

Thank you!